TP9500/TP9600 Portable Radios

Operational Description

TD-0058-01 · Issue 1 · December 2019

Contact Information

Tait Communications
Corporate Head Office

Tait International Limited
P.O. Box 1645
Christchurch
New Zealand

For the address and telephone number of regional offices, refer to our website: www.taitradio.com

Copyright and Trademarks

Disclaimer

There are no warranties extended or granted by this document. Tait International Limited accepts no responsibility for damage arising from use of the information contained in the document or of the equipment and software it describes. It is the responsibility of the user to ensure that use of such information, equipment and software complies with the laws, rules and regulations of the applicable jurisdictions.

Enquiries and Comments

If you have any enquiries regarding this document, or any comments, suggestions and notifications of errors, please contact your regional Tait office.

Updates of Manual and Equipment

In the interests of improving the performance, reliability or servicing of the equipment, Tait International Limited reserves the right to update the equipment or this document or both without prior notice.

Intellectual Property Rights

This product may also be made under license under one or more of the following patents:
- US7203207, AU2004246135, CA2527142, GB2418107, HK1082608, MY134526, US8306071
- US7339917, AU2004246136, CA2526926, GB2418812, MY134217
- US7499441, AU2005262626, CA2570441, GB2430333, JP4690397, NZ551231, KR100869043, RU2351080, BRP10512052, MXPA06015241
- US 7200129, AU2005226531, CA2558551, CN1930809, GB2429378, JP4351720, BRP10508671, NZ549124, KR848483, RU2321952

The Bluetooth® word mark and logos are registered trademarks owned by Bluetooth SIG, Inc, and any use of such marks by Tait International Limited is under licence. Other trademarks and trade names are those of their respective owners.

To Our European Customers

Tait International Limited is an environmentally responsible company which supports waste minimization, material recovery and restrictions in the use of hazardous materials.

The European Union's Waste Electrical and Electronic Equipment (WEEE) Directive requires that this product be disposed of separately from the general waste stream when its service life is over. For more information about how to dispose of your unwanted Tait product, visit the Tait WEEE website at www.taitradio.com/weee. Please be environmentally responsible and dispose through the original supplier, or contact Tait International Limited.

Tait International Limited also complies with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive in the European Union.

In China, we comply with the Measures for Administration of the Pollution Control of Electronic Information Products. We will comply with environmental requirements in other markets as they are introduced.

1 Introduction

The TP9500/TP9600 series is a range of high-performance microprocessor-controlled radios for voice and data communication.

Main Items of System

The TP9500/TP9600 series is capable of digital, analog and mixed operation. The system consists of the following main items:

- radio
- antenna
- battery
- battery charger
- audio accessories

The service manual covers the servicing of the radio and battery chargers, and describes how to troubleshoot the battery.

Radio

The radio body contains the transmitter, receiver and microprocessor circuitry. There are two standard external connectors on the radio body: an antenna connector and an accessory connector. The accessory connector allows the connection of various external devices to the radio.

User interface

All radios have a power/volume control, a 3-way selector control and a programmable key on the top of the radio, the PTT key, and three function keys at the side of the radio. The front panel has an LCD on the front panel, two scroll keys, two selection keys and 12 alphanumeric keys.

Frequency Bands

The radios are available in the following frequency bands:

Frequency code	Frequency band
B1	136 MHz to 174 MHz
H7	450 MHz to 520 MHz
HK	378 MHz to 470 MHz
K5	757 MHz to 870 MHz (Tx) 757 MHz to 776 MHz (Rx) 850 MHz to 870 MHz (Rx)

A different RF board is used to implement each band; the rest of the radio remains the same.

RF Output Power

This table shows the RF power output when the radio is operated at each of the available frequency bands.

		B1	H7, HK	K5
	High	5W	4W	3W
	Medium	3W	2.5W	2.5W
	Low	2W	2W	2W
	Very low	1W	1W	1W

Audio Accessories

One audio accessory can be connected to the accessory connector of the radio body. Tait offers a range of speaker microphones and headsets.

Antennas

A range of wide-band antennas and mini-helical antennas for a limited frequency range are available.

Batteries

The following Lithium-ion batteries are available:

- 1880 mAh ('slimline')
- 2400 mAh ('performance')

Battery Chargers

The following battery chargers are available:

- single Lithium-ion desktop charger
- six-way Lithium-ion multicharger
- battery-only in-vehicle charger
- in-vehicle charger

Carry Accessories

A range of holsters and a belt clip are available.

2 General Description

2.1 Hardware and Software Architecture

The interaction of hardware and software modules enables the radio to function.

2.1.1 Hardware Architecture

The electrical hardware of the radio is implemented on two boards: a main board and an MMI board. The two boards are connected by a flexible loom.

Main Board

The main board inside the radio body includes the following:

- Transmitter circuitry
- Receiver circuitry
- Frequency synthesizer circuitry
- Digital circuitry with a RISC processor and custom logic (implemented on an FPGA), memory, and a DSP
- CODEC and audio circuitry
- Interface circuitry
- Power supply circuitry

For a basic block diagram of the main board, refer to Figure 1 on page 6.

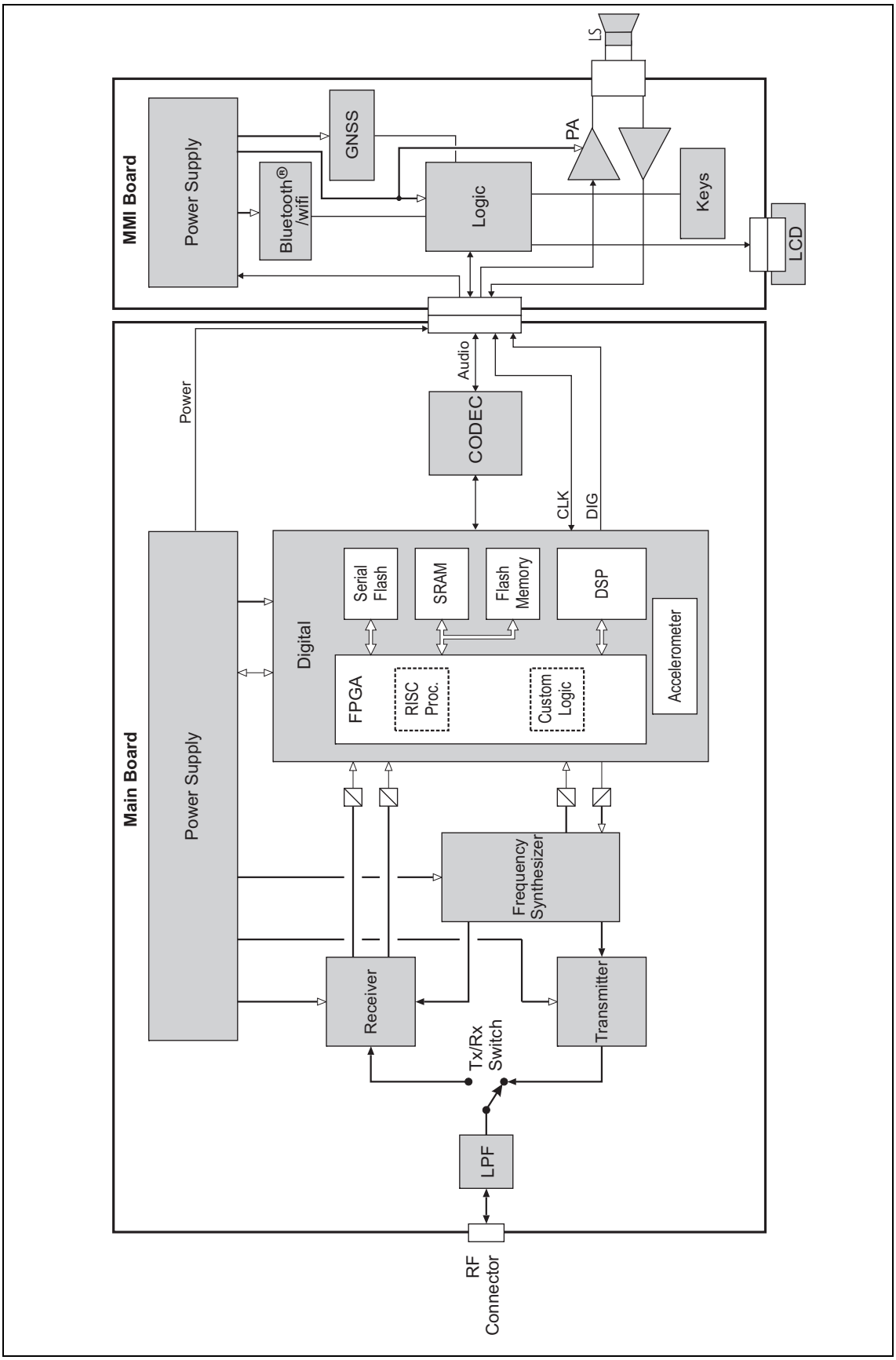
For a more detailed block diagram of the transceiver, refer to Figure 3 on page 11 (analog mode) and Figure 4 on page 12 (digital mode).

MMI Board

The MMI board includes the following:

- User interfaces circuitry
  For a description of the radio controls, refer to “User interface” on page 3.
- Graphical LCD module
- Global Navigation Satellite System (GNSS)
- Bluetooth®/wifi module

Figure 1 Hardware architecture of the main board and MMI board



2.1.2 Software Architecture

Overview

Software plays an important role in the functioning of the radio. Some radio functions such as the graphical user interface, processing of the analog and digital signals, and the implementation of radio applications are completely implemented by software.

For a block diagram of the software architecture, refer to Figure 2 on page 8.

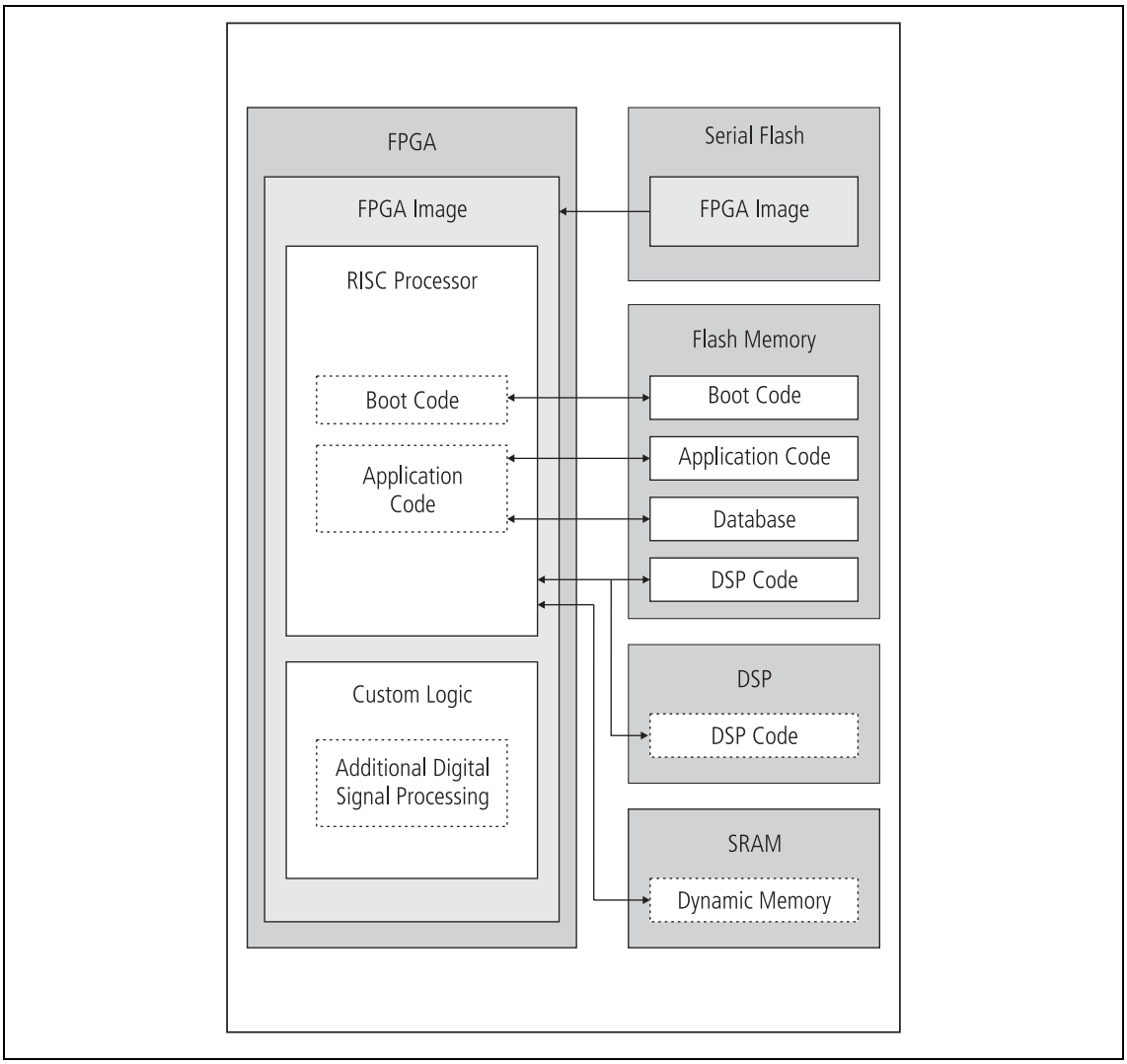
Software Modules

The following software modules are stored on the digital sub-system of the main board:

- FPGA image, which includes the software-implemented RISC processor and the custom logic (the custom logic executes additional digital signal processing)
- boot code
- radio application code
- digital signal processing
- radio application database and radio calibration database

Hardware and interface drivers are part of the boot code, the RISC code, and—in the case of the main board—the DSP code.

Figure 2 Software architecture (radio with graphical-display control head shown)



Software Start-Up When the radio is turned on, the following processes are carried out:

This process describes the software start-up into normal radio operation mode.

1. The FPGA image, which includes the RISC processor and the custom logic, is loaded from the serial flash to the FPGA.
2. The RISC processor executes the startup sequence, which carries out an initialization and auto-calibration, and—in the case of a fault—generates an error code for display on the LCD.
3. Normal radio operation starts with:
   - the RISC processor executing the radio application code, including application software
   - the DSP executing the DSP code for processing of digital signals
   - the custom logic executing additional digital signal processing

Software Shutdown

On shutdown, the programming and calibration data is stored in the database, and power is removed from the radio.

> **Notice** On power loss, any changes made to the programming or calibration data may be lost.

Programming and Calibration Files

One of the servicing tasks is the downloading and uploading of programming and calibration files to the database. For more information, refer to the Help of the programming and calibration applications.

Software Upgrades

During servicing it may become necessary to upload software to a replacement main board, using the **Tools** > **Download** command of the programming application. For more information, refer to the Help of the programming application and to the technical notes accompanying the software files.

2.2 Operation in Receive Mode

Overview

This section describes the functioning of the transceiver in receive mode.

The operation of the transceiver is illustrated in Figure 3 on page 11 (analog mode) and Figure 4 on page 12 (digital mode).

These block diagrams show the hardware modules integrated with the software modules:

- hardware (transmitter, receiver, frequency synthesizer, CODEC and audio)
- RISC processor (on FPGA of digital sub-system)
- custom logic (on FPGA of digital sub-system)
- DSP

The block diagrams for the analog and digital modes only differ in the operation of the DSP.

The receive path consists of three major functional parts:

- RF hardware
- digital down-conversion and baseband processing
- audio processing and signaling

The information flow on a digital radio can be categorized in two forms, signaling (including user data) and voice. While setting up a call, signaling may be the only information transferred across the air interface. Once a call has been established however, both signaling and voice information are transported. The signaling information continues throughout the call for the purpose of maintaining the call and possibly sending data information.

Figure 3 Transceiver operation in analog mode

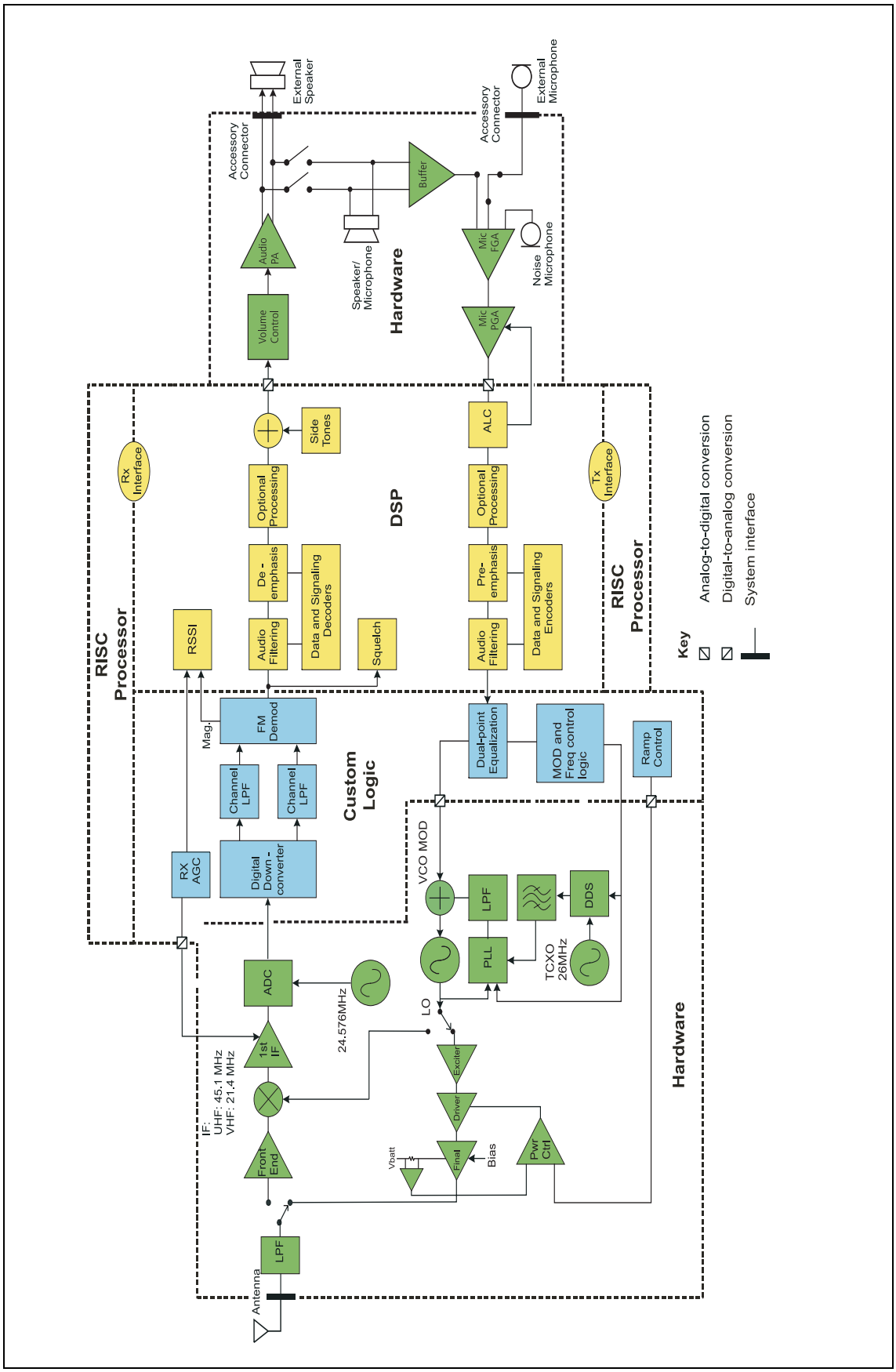
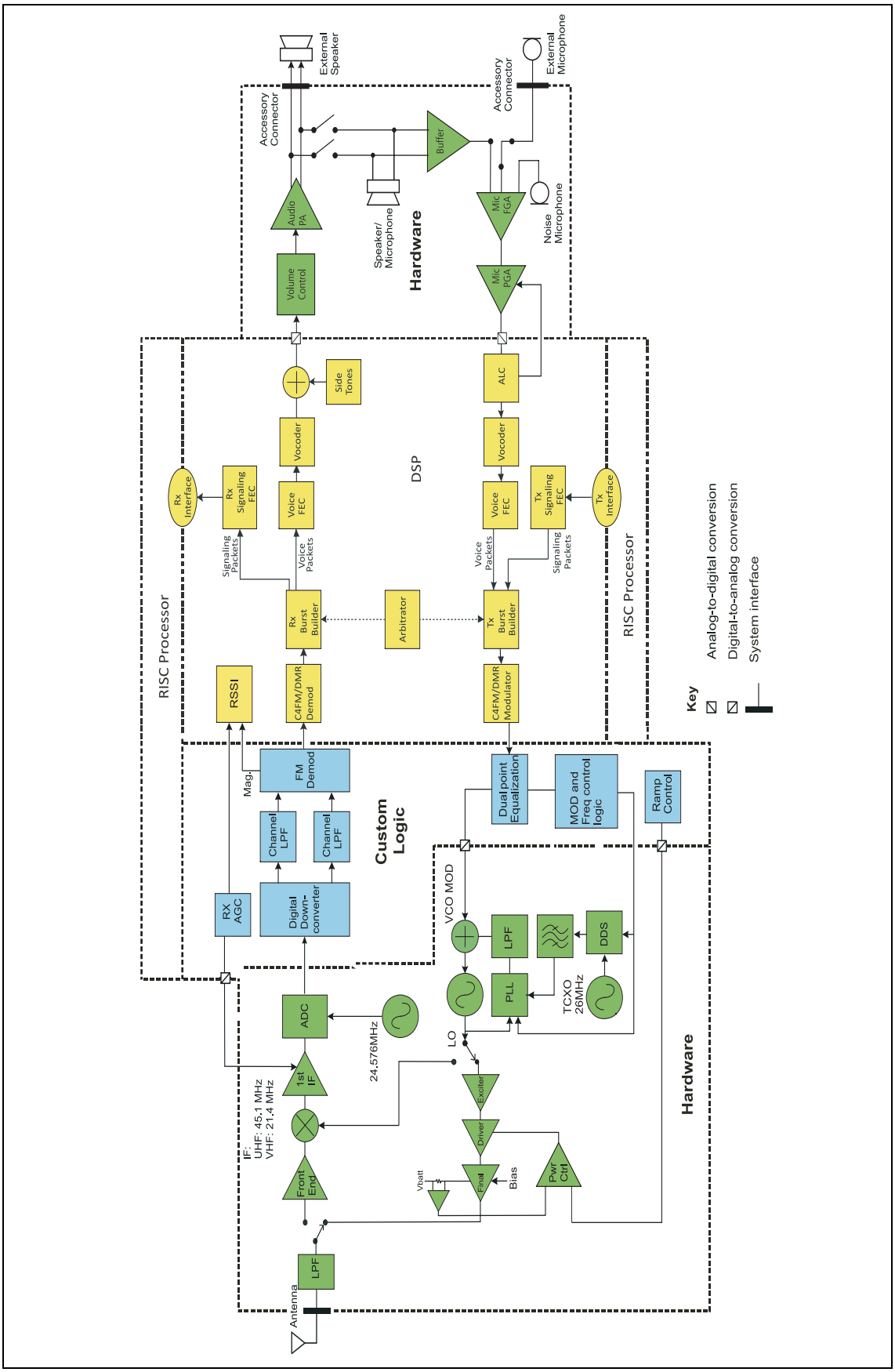


Figure 4 Transceiver operation in digital mode



2.2.1 RF Hardware

Tx-Rx Switch

The Tx-Rx switch circuitry selects the RF path to and from the antenna to either the Tx or Rx circuitry of the radio. In addition to the switching functionality, the switch is used to provide attenuation to the Rx front end in high signal-strength conditions.

Front End and First IF

The front-end hardware amplifies and image-filters the received RF spectrum, then down-converts the desired channel frequency to a first intermediate frequency (IF1) of 21.4 MHz (VHF) or 45.1 MHz (UHF), where coarse channel filtering is performed. Front-end image filtering is performed using tunable filters at VHF and switched, fixed-frequency filters at UHF. The first LO signal is obtained from the frequency synthesizer and is injected on either the high side (K5 from 757 to 776 MHz) or the low-side (B1, H7, HK, K5 from 850 to 870 MHz, L3) of the desired channel frequency. In receive mode, the modulation to the frequency synthesizer is muted. See "Frequency Synthesizer" on page 19 for a description of the frequency synthesizer. The IF signal is amplified through IF and AGC amplifiers, after which it is subsampled directly using a high speed ADC, sampling at a nominal frequency of 24.576 MHz.

The remainder of the down-conversion and processing is performed in custom logic and DSP.

Automatic Gain Control

The AGC is used to limit the maximum signal level applied to the ADC in order to meet the requirements for intermodulation and selectivity performance. Hardware gain control is performed by a variable gain amplifier driven by a 10-bit DAC.

Information about the signal level is obtained directly from the subsampled ADC output. The control loop is completed within the custom logic. The AGC will begin to reduce gain when the combined signal power of the wanted signal and first adjacent channels is greater than about -70 dBm. In the presence of a strong adjacent-channel signal it is therefore possible that the AGC may start acting when the wanted signal is well below -70 dBm.

2.2.2 Digital Down-conversion and Baseband Processing

Custom Logic

The subsampled received signal from the high speed ADC is digitally down-converted in custom logic to baseband via a second IF of 768 kHz. The first stage of this digital down-conversion is performed using a high side or low side NCO for VHF and UHF, respectively. The signal is then filtered and decimated to reduce the sampling rate from 24.576 MHz to 6.144 MHz before converting to baseband using a quadrature mixer. The LO for the quadrature mixer is derived by a divide-by-32 of the digital system clock (24.576 MHz).

After mixing to baseband, the signal is further decimated to reduce the sample rate to 48 kHz before performing channel filtering and demodulation. Different channel filter shapes are possible to accommodate the various channel spacings and data requirements. These filters provide the bulk of adjacent channel selectivity for narrow-band operation. The filters have linear phase response so that good group-delay performance for data is achieved. Custom logic also performs demodulation, and the demodulated signal is then multiplexed with amplitude data and fed via a single synchronous serial port to the DSP. The stream is demultiplexed and the demodulation data used as an input for further audio processing.

Noise Squelch

The noise squelch process resides in the DSP. The noise content above and adjacent to the voice band is measured and compared with a preset threshold. When a wanted signal is present, out-of-band noise content is reduced and, if below the preset threshold, is indicated as a valid wanted signal.

RSSI

Receive signal strength is measured by a process resident in the DSP. This process obtains its input from the demodulator (RF signal magnitude value) and from the AGC (present gain value). With these two inputs and a calibration factor, the RF signal strength at the antenna can be accurately calculated.

Calibration

The following items within the receiver path are factory-calibrated:

- front-end tuning
- AGC gain curve
- noise squelch
- RSSI
- Gain correction factors (frequency dependant)

Information on the calibration of these items is given in the Help of the calibration application.

2.2.3 Audio Processing and Signaling

Audio Processing (Analog Mode)

Raw demodulated data from the receiver is processed within the DSP. The sample rate at this point is 48kHz with signal bandwidth limited only by the IF filtering. Scaling (dependent on the bandwidth of the RF channel) is then applied to normalize the signal level for the remaining audio processing. The sample rate is decimated to 8kHz and 0.3 to 3kHz bandpass audio filtering is applied. De-emphasis is then applied to cancel out the receive signals pre-emphasized response and improve signal to noise performance. Optional processing such as decryption or companding is then applied if applicable.

Data and Signaling Decoders (Analog Mode)

The data and signaling decoders obtain their signals from various points within the audio processing chain. The point used depends on the decoders' bandwidth and whether de-emphasis is required. Several decoders may be active simultaneously.

Side Tones

Side tones are summed in at the end of the audio processing chain. These are tones that provide some form of alert or give the user confidence an action has been performed. The confidence tones may be generated in receive or transmit mode. The sidetone level is a fixed proportion (in the order of -10dB) relative to full scale in the receive path.

C4FM and DMR Demodulators (Digital Mode)

Once the received signal is FM demodulated, it enters either the C4FM or the DMR de-modulator, depending on the radio configuration. Once synchronization has been acquired, the received signals should exist as four possible frequencies. These frequencies are translated directly into received symbols ready to be passed to the burst builder.

Rx Burst Builder (Digital Mode)

The job of the burst builder is to dismantle the received burst. The burst builder can only receive an incoming burst once synchronization has been achieved by the C4FM or DMR modems. The synchronization sequence itself does not contain meaningful signaling payload and is discarded by the burst builder. The payload content of the burst is dismantled and routed to the appropriate signaling FEC or voice FEC task for decoding.
The dismantling process is the reverse of the construction process performed by the burst builder.

Rx Signaling FEC (Digital Mode)

Prior to transmission, signaling information such as the network identifier was protected with forward error correction. Upon reception, the signaling may contain errors. If the number of errors is limited they can be corrected to recover the originally transmitted signaling.

Rx Vocoder FEC (Digital Mode)

The bits received from the burst builder are de-interleaved on a frame by frame basis. An attempt is made to decode the vocoder bits using the complementary process to that used in the encoder. An indication of the success of the decoder is produced. If the FEC algorithm is unable to

decode correctly, a recommendation is made to the vocoder, depending on the severity of the errors, to either guess what the frame should be, to repeat the last frame, or to mute for this frame.

Rx Vocoder (Digital Mode)

The bits from the FEC are decoded to generate the fundamental frequency of the frame, the voiced/unvoiced decisions for each frequency band, and the spectral amplitudes. 20ms of speech is synthesized from this information, and is interpolated between the previous frame and the next frame to minimize any artefacts due to the transition from one frame to the next.

Audio PA

The combined audio and side-tone signal is converted to analog form by the audio PA.

The output configuration of the audio power amplifier is balanced and drives an internal speaker and, optionally, an external speaker. The speaker loads are connected in parallel but the internal speaker can be switched under software control. The power delivered to each speaker is limited by its impedance. The internal speaker has 8Ω impedance whereas the external speaker can be higher than this.

2.3 Operation in Transmit Mode

Overview

This section describes the functioning of the transceiver in transmit mode.

The operation of the transceiver is illustrated in Figure 3 on page 11 (analog mode) and Figure 4 on page 12 (digital mode).

These block diagrams show the hardware modules integrated with the software modules:

- hardware (transmitter, receiver, frequency synthesizer, CODEC and audio)
- RISC processor (on FPGA of digital sub-system)
- custom logic (on FPGA of digital sub-system)
- DSP block

The block diagrams for the analog and digital modes only differ in the operation of the DSP.

The transmit path consists of three major functional parts:

- audio processing and signaling
- frequency synthesizer
- RF transmitter

The information flow on a digital radio can be categorized in two forms, signaling (including user data) and voice. Whilst setting up a call, signaling may be the only information transferred across the air interface. Once a call has been established however, both signaling and voice information are transported. The signaling information continues throughout the call for the purpose of maintaining the call and possibly sending data information.

2.3.1 Audio Processing and Signaling

Microphone Input

The input to the transmitter path begins at the microphone input. There are three microphone sources: the internal speaker/microphone, an internal noise microphone, and an accessory microphone connected via the accessory connector. Only electret-type microphones are supported.

Analog Processing of the Microphone Input

The CODEC performs microphone selection and amplification.
The microphone amplifier consists of a programmable-gain amplifier with 0 to 54dB gain. The amplified microphone signal is converted to a digital stream by a 16-bit ADC with integral anti-alias filtering (0.1 to 3.2kHz). The digital stream is transported to the DSP for further audio processing.

Automatic Level Control

The ALC follows and is used to effectively increase dynamic range by boosting the gain of the microphone pre-amplifier under quiet conditions

and reducing the gain under noisy acoustic conditions. The ALC function resides in the DSP and controls the microphone-programmable gain amplifier in the CODEC. The ALC has a fast-attack (about 10 ms) and slow-decay (up to 2 s) gain characteristic. This characteristic ensures that the peak signal level is regulated near full scale to maximize dynamic range.

Active Noise Cancelation

Optional processing uses a pair of microphones (internal microphone plus noise microphone, or accessory microphone plus internal microphone) to isolate the users' voice from the background noise.

DSP Audio Processing (Analog Mode)

The output of the automatic level control provides the input to the DSP audio processing chain at a sample rate of 8 kHz. Optional processing such as encryption or companding is done first if applicable. Pre-emphasis, if required, is then applied. The pre-emphasized signal is hard limited to prevent over-deviation and filtered to remove high frequency components. The sample rate is then interpolated up to 48 kHz and scaled to be suitable for the frequency synthesizer.

Data and Signaling Encoders (Analog Mode)

The data and signaling encoders inject their signals into various points within the audio processing chain. The injection point depends on the encoders bandwidth and whether pre-emphasis is required.

Tx Vocoder (Digital Mode)

The AMBE vocoder block takes audio samples in blocks of 20 ms, analyses them and compresses them down to 88 bits. If there is no speech content in the segment, the vocoder produces silence. If speech is detected in the segment, the content of the segment is split into a variable number of frequency bands (max. 12) and a voiced/unvoiced decision is made for each band. It also estimates the pitch of the segment of speech and determines the spectral amplitudes of the voiced frequency bands.

Tx FEC (Digital Mode)

Voice, data, and signaling information is protected using forward error correction.

Tx Burst Builder (Digital Mode)

It is the nature of a digital radio transmission that the information is structured into bursts. An air interface burst can take several forms. Bursts consist of a frame synchronization sequence and/or payload, the exact content of which depends upon the type of burst. For a voice burst, it comprises a fixed number of voice packets with control signaling and low speed data interspersed. For a data or control burst, it comprises a variable number of data blocks.

It is the job of the burst builder to construct the air interface burst using FEC-encoded code words delivered to it by the signaling FEC and voice FEC. The burst is then passed to the C4FM or DMR modulator.

C4FM/DMR Modulator (Digital Mode)

The burst builder creates a symbol stream that must be modulated onto the RF carrier, for the desired modulation scheme. They are passed through a shaping filter defined by the APCO and DMR standards, which limit the spectral occupancy on air.

2.3.2 Frequency Synthesizer

Introduction

As shown in Figure 3, the frequency synthesizer consists of two main parts:

- TCXO and DDS reference and its output filter
- RF PLL, comprising RF PLL device, loop filter, VCO, and VCO output switch Frequency reference

Frequency Reference

The frequency reference consists of the following:

- TCXO
- DDS
- frequency control block

The DDS provides the reference frequency for the RF PLL.

RF PLL

The RF PLL consists of the following:

- RF PLL device
- loop filter
- VCO
- VCO output switch

Operation of PLL Control Loop

The RF PLL is a single loop fractional “N” synthesiser based design. The PLL reference is obtained from the DDS IC that is clocked by the 26MHz ± 0.5 ppm TCXO. The DDS output frequency is set at approximately 10.7MHz and divided by the R counter of the PLL by 5, thus the phase detector frequency is around 2.14MHz. The VCO output is sampled and fed back to the PLL RF pre-scaler input. The PLL and DDS is programmed on each and every frequency change i.e. RX to TX, TX to RX, RX to RX.

The loop filter is an active type allowing a control voltage range of up to 15volts to the VCO control line. The VCO covers both the RX and TX frequencies and has a positive frequency with control volts transfer function.

Modulation

This PLL subsystem has dual-point modulation applied, in analog form, to only the VCO and in digital form to the DDS IC. The DDS output is filtered by analogue filters and has FM modulation on the filtered reference. The combination of the reference to the synthesizer with scaled analogue modulation to the VCO results in a flat FM modulation response from DC to 3kHz. The DDS IC is continually updated at a rate of 12.288MHz during

transmit with the modulation frequency and deviation information, and remains static in receive mode.

Frequency Generation

The RF PLL has a frequency resolution due to the fractional N synthesizer of some few milliHertz. Thus all channels can be programmed down to the small increments required such as 2.5kHz. The single VCO output is amplified, lowpass filtered and applied by a RF switch to the TX exciter input in transmit mode and to the RX mixer LO input in receive mode.

Frequency Acquisition of RF PLL

In the RF PLL the loop bandwidth is initially set to maximum by increasing the charge-pump current to its maximum for a specified period and then reducing the current to a lower steady state value. As a result, settling to within ±100Hz of the final frequency value occurs in under the minimum specified time for the operation of the digital modulation system.

Calibration

The following items are programmed and calibrated in the frequency generation subsystem.

- VCO frequency
- VCO deviation
- DDS frequency, modulation frequency and deviation

2.3.3 RF Transmitter

RF Power Amplifier and Switching

The RF power amplifier is a four-stage line-up with approximately 32dB of power gain. The output of the frequency synthesizer is first buffered to reduce kick during power ramping. The buffer output goes to a broadband exciter IC that produces approximately 100mW output. The exciter is followed by an LDMOS driver producing up to 1W output, followed by the final stage which consists of a single LDMOS device, producing enough power to provide 3W, 4W or 5W at the antenna.

Output of RF Power Amplifier

The output of the RF power amplifier passes through the Tx-Rx switch. The Tx-Rx switch toggles the antenna path between the receiver and transmitter in receive and transmit modes respectively. Finally, the output is low-pass-filtered to bring harmonic levels within specification.

Power Control

The steady-state power output of the transmitter is regulated using a hardware control loop. The DC current drawn by the final PA device is sensed and amplified, and then feeds into the power control loop integrator. The power control signal is supplied by a 10-bit DAC driven by custom logic. This power control voltage feeds the gate of the driver device, to perform the power control.

The gate of the driver device is hardware clamped to prevent overdrive of the final device. Under load mismatch (VSWR), the current drawn by the

PA is maintained and the output power allowed to vary within predetermined limits.

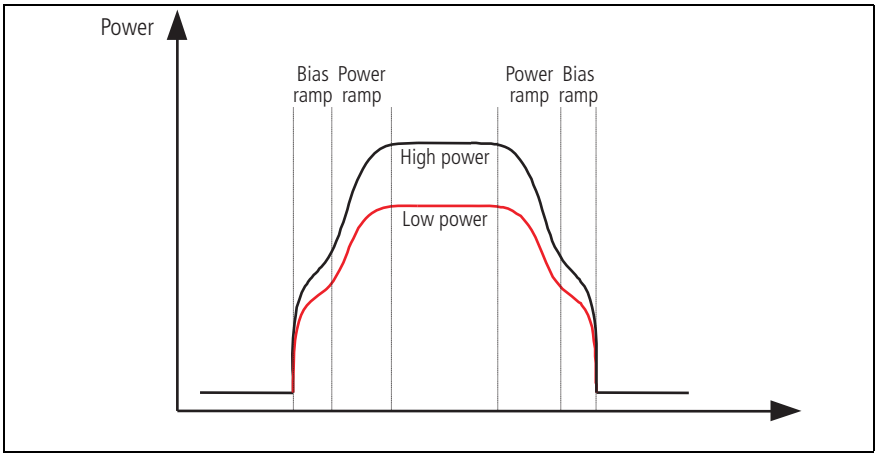
Ramping

Power ramp-up consists of two stages:

- bias
- power ramping

The timing between these two stages is critical to achieving the correct overall wave shape in order to meet the specification for transient ACP (adjacent channel power). A typical ramping waveform is shown in Figure 5.

Figure 5 Typical ramping waveforms



Bias Ramp-Up

The steady-state final and driver-clamp bias levels are supplied by a 10-bit DAC programmed prior to ramp-up but held to zero by a switch on the DAC output under the control of a TX INHIBIT signal. Bias ramp-up begins upon release by the TX INHIBIT signal with the ramping shape being determined by a low-pass filter. Owing to power leakage through the PA chain, ramping the bias takes the PA output power to approximately 30 dB below steady-state power.

Power Ramp-Up

The power ramp signal is supplied by a 10-bit DAC that is controlled by custom logic. The ramp is generated using a look-up table in custom logic memory that is played back at the correct rate to the DAC to produce the desired waveform. The ramp-up and ramp-down waveforms are produced by playing back the look-up table in forward and reverse order respectively. For a given power level the look-up table values are scaled by a steady-state power constant so that the ramp waveform shape remains the same for all power levels.

Tx-Rx Switch

The Tx-Rx switch circuitry selects the RF path to and from the antenna to either the Tx or Rx circuitry of the radio. In addition to the switching functionality, the switch is used to provide attenuation to the Rx front end in high signal-strength conditions.

3 Circuit Block Diagrams

List of Diagrams

Block diagrams in this section show the modules of the main board, and the front-panel interface board:

Figure 1 Block diagram of the receiver circuitry

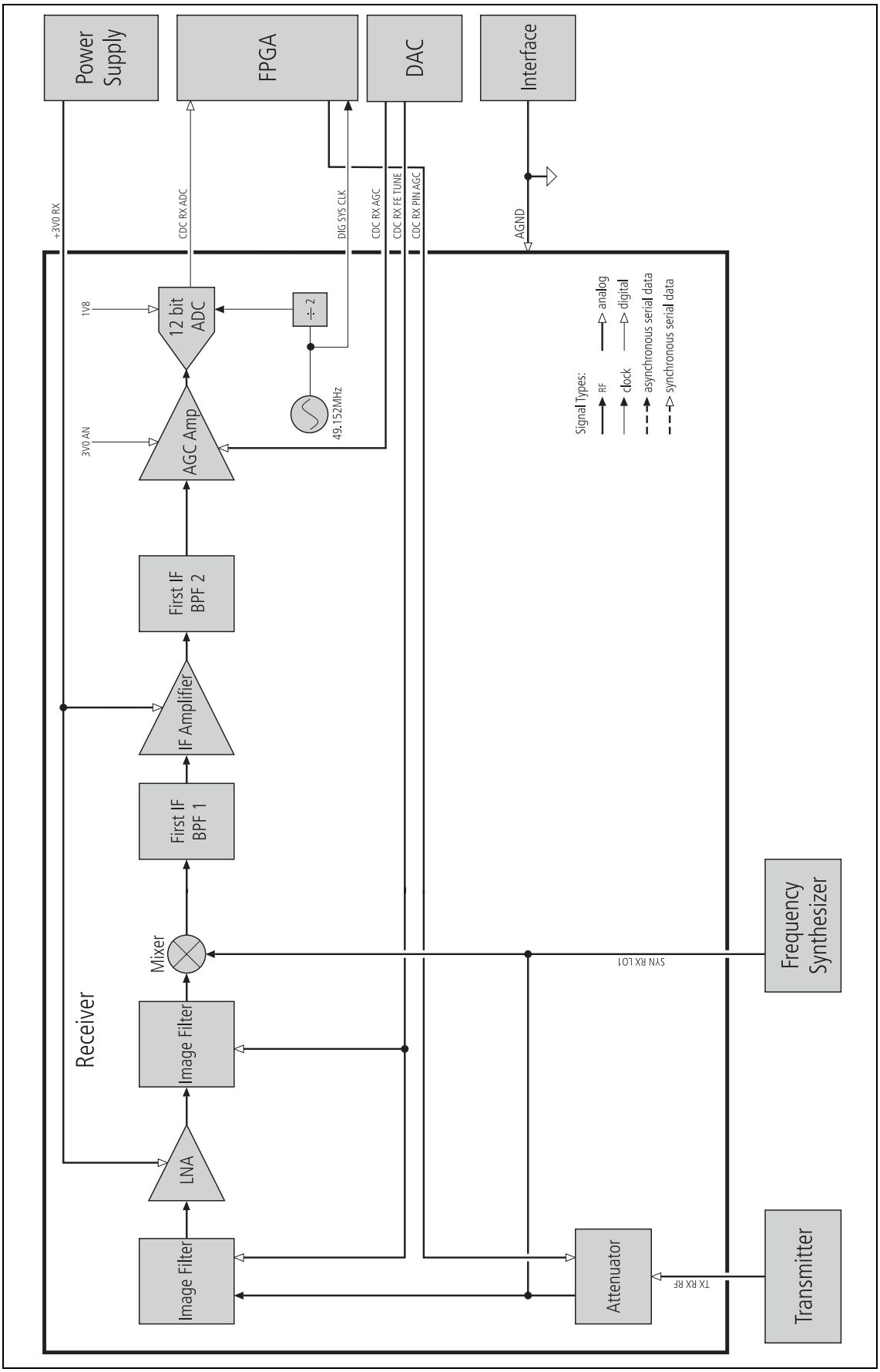


Figure 2 Block diagram of the transmitter circuitry

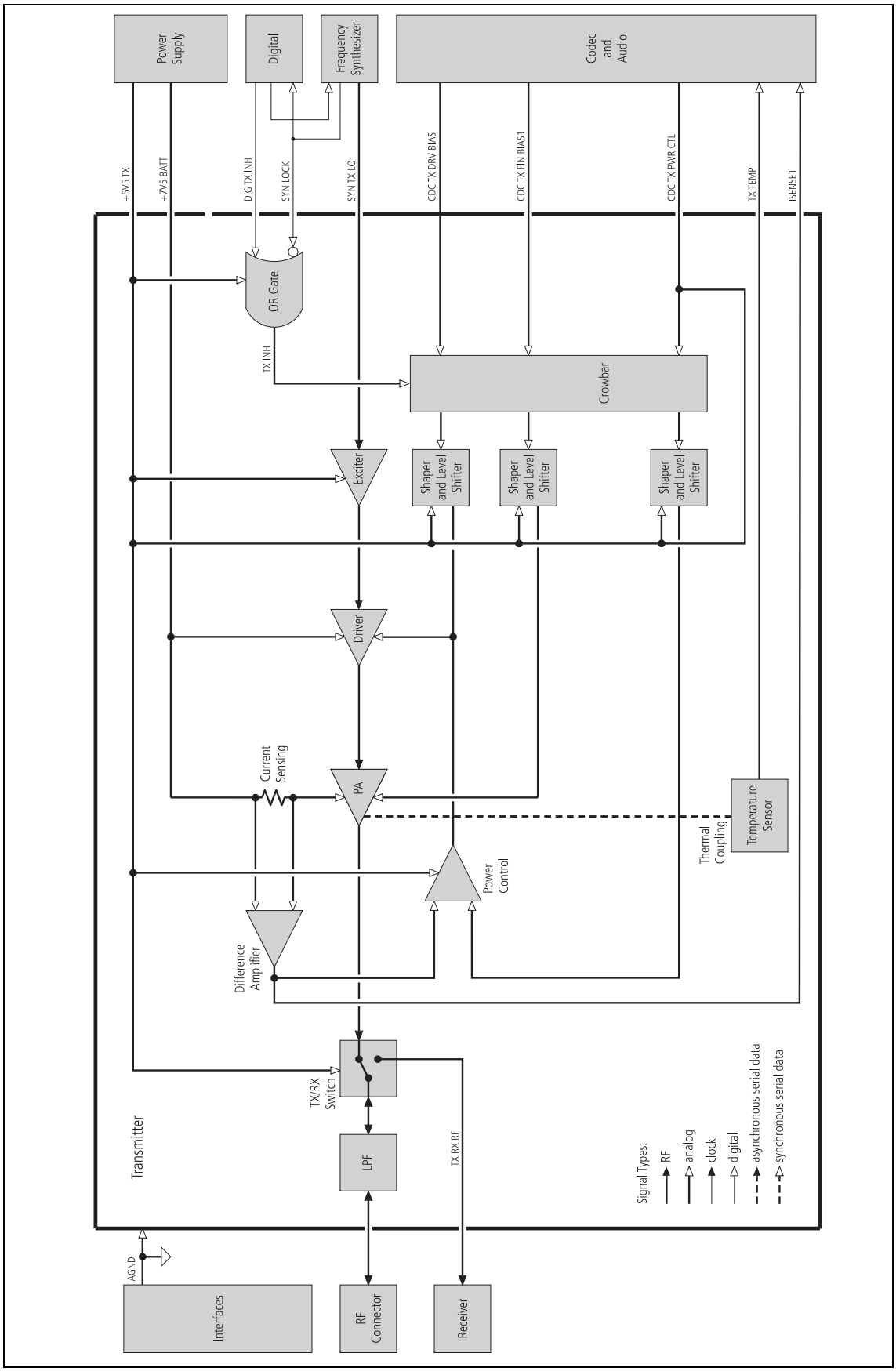


Figure 3 Block diagram of the frequency synthesizer circuitry

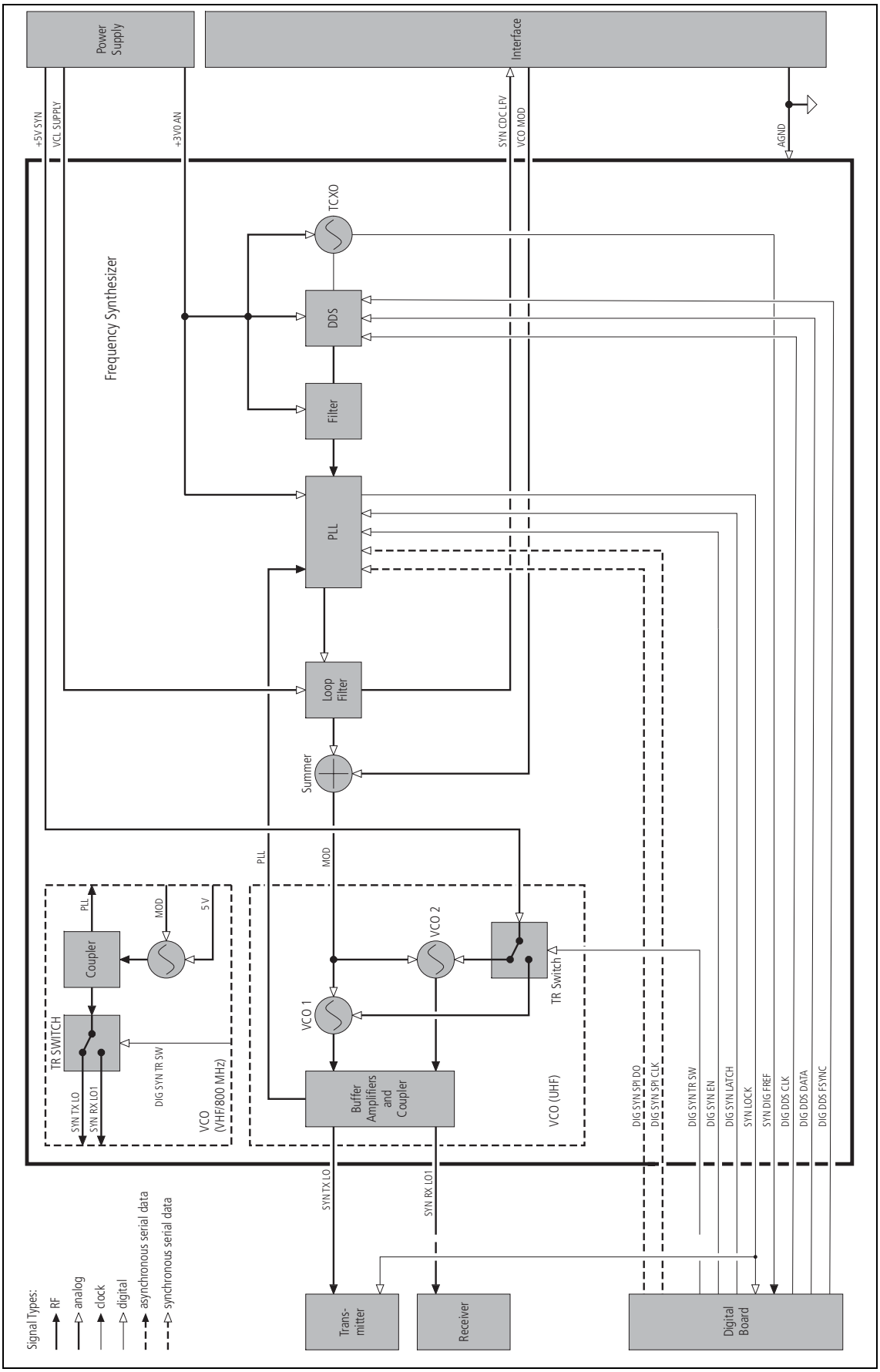


Figure 4 Block diagram of the CODEC and audio circuitry

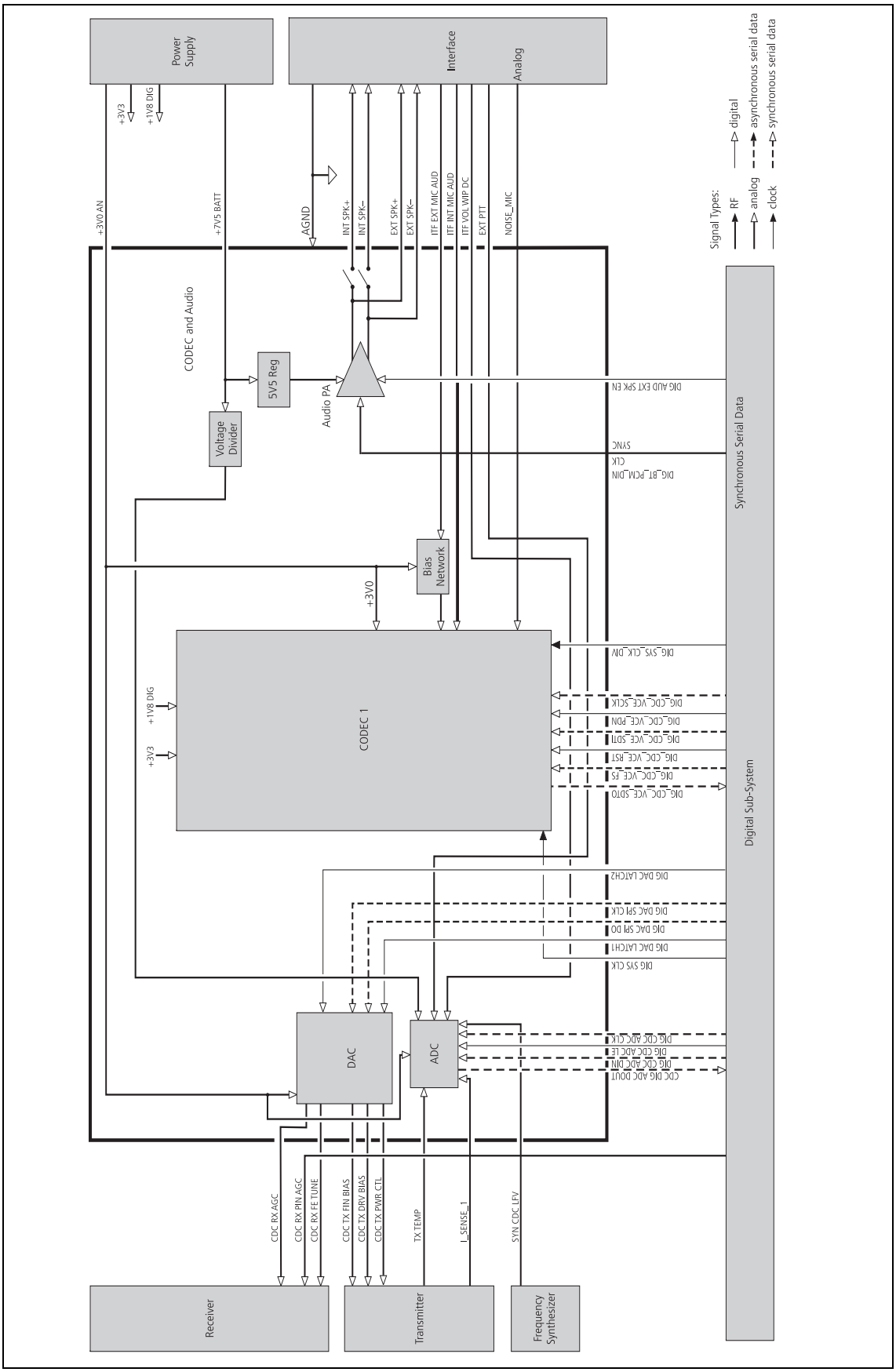


Figure 5 Block diagram of the power supply circuitry

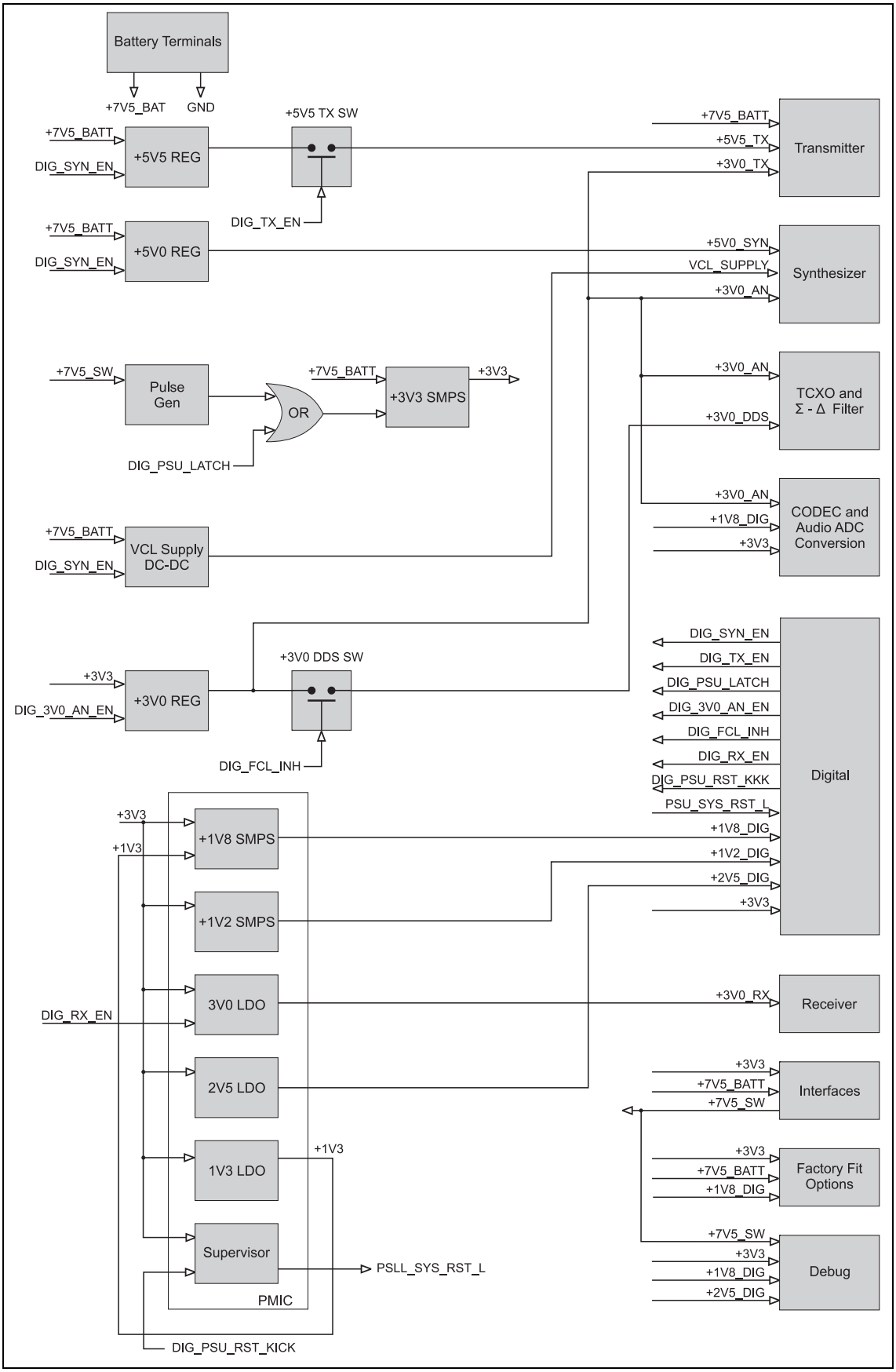


Figure 6 Block diagram of the main board

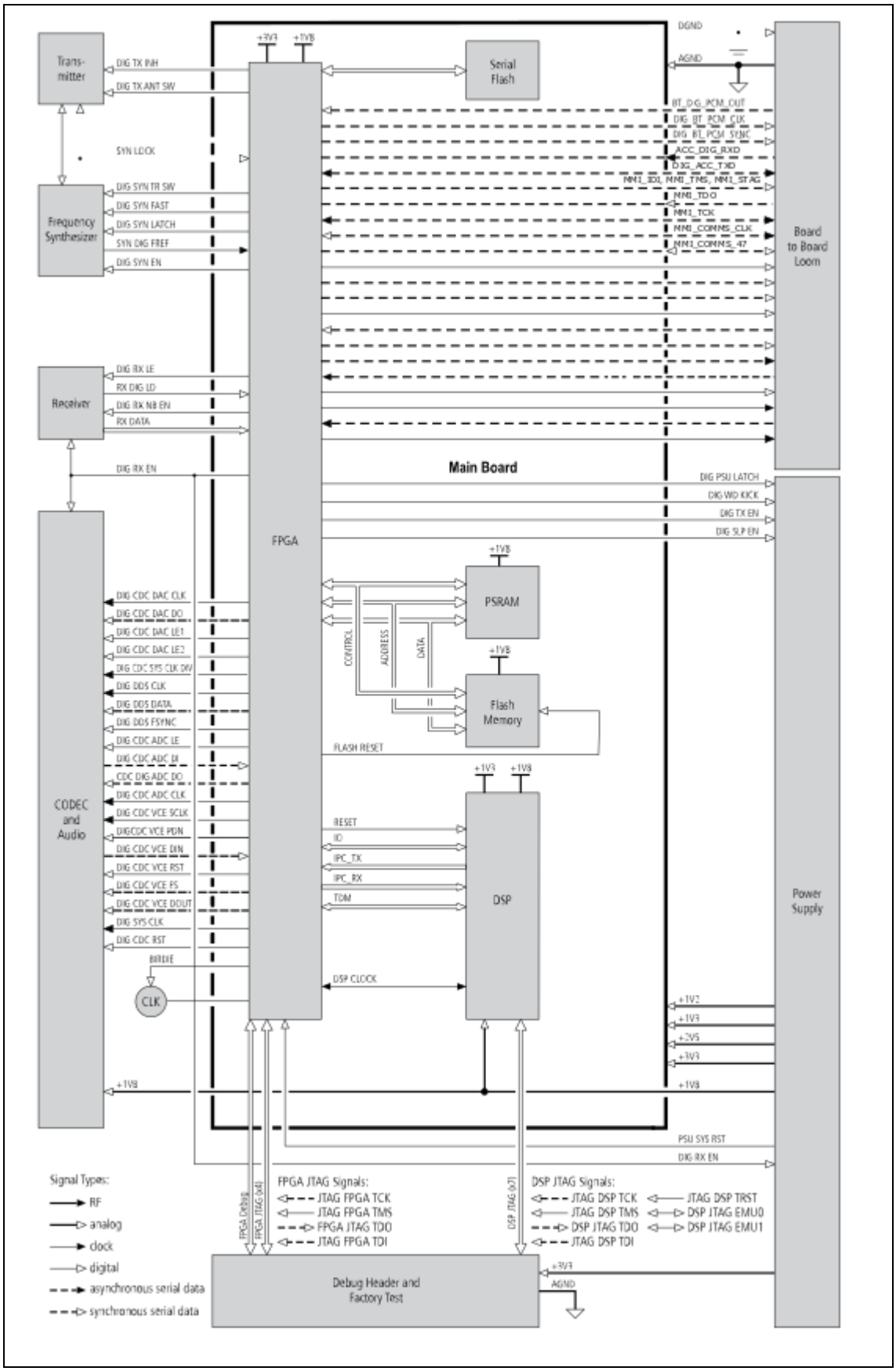


Figure 7 Block diagram of the MMI